REMARKS

The application has been reviewed in light of the Office Action mailed on July 9, 2010. Claims 1-14 are currently pending in the application, with claims 1 and 14 being in independent form. By the present Amendment, claim 3 has been canceled and claims 1-2, 4, 6, 9 and 13-14 have been amended. Support is found at least in paragraphs [32-33, 35, 37, 42-43, 45-46, 48 and 52-54] and FIG. 8 of the specification and canceled claim 3. No new matter has been added. It is respectfully submitted that the claims pending in the application, namely claims 1-2 and 4-14 are patentable over the prior art.

The present invention is directed to a process for manufacturing a silicon-on-insulator wafer. A silicon substrate is provided. An oxide insulator layer is formed across the wafer by oxygen implantation. The insulator layer is buried within the silicon substrate. The insulator layer includes a top surface and a bottom surface. The insulator layer divides the silicon substrate from a top silicon layer. The insulator layer is thickened by reducing one or more of the implantation dose, energy, and temperature. At least one of a contoured top surface and a contoured bottom surface of the insulator layer are created by adjusting one or more of the implantation dose, energy, and temperature. Annealing is performed to further thicken and contour the insulator layer.

Objection to Claims 1-14

Claims 1-14 are objected to for informalities. All of the element digits in claims 1-2, 4, 6, 9 and 13-14 were removed.

Rejection of Claims 1, 3-5, 7-8, 11-12 and 14 under 35 U.S.C. § 103(a)

Claims 1, 3-5, 7-8, 11-12 and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Forbes (U.S. Patent No. 7,262,428), hereinafter "Forbes" in view of Yamagata

(U.S. Patent No. 6,653,209), hereinafter "Yamagata". Claim 1 has been amended in a manner believed to overcome the rejection. In particular, claim 1 has been amended to recite "forming an oxide insulator layer across the wafer by oxygen implantation, the insulator layer being buried within the silicon substrate, dividing the silicon substrate from a top silicon layer, and having a top surface and a bottom surface", "thickening the insulator layer by reducing one or more of the implantation dose, energy, and temperature" and "creating at least one of a contoured top surface and a contoured bottom surface of the insulator layer by adjusting one or more of the implantation dose, energy, and temperature". Support is found at least in paragraphs [32-33, 35, 37, 42-43, 45-46, 48 and 52-54] and FIG. 8 of the specification and canceled claim 3.

Forbes does not disclose or suggest "forming an oxide insulator layer across the wafer by oxygen implantation, the insulator layer being buried within the silicon substrate, dividing the silicon substrate from a top silicon layer, and having a top surface and a bottom surface", "thickening the insulator layer by reducing one or more of the implantation dose, energy, and temperature" and "creating at least one of a contoured top surface and a contoured bottom surface of the insulator layer by adjusting one or more of the implantation dose, energy, and temperature". Referring to column 7, lines 46-51 and FIG. 1F, Forbes teaches processing a substrate 110 to form a strained Si/SiGe/SOI island. A bubble recess 132 is formed by an isotropic etch and "an oxidation process is carried out to vertically isolate an SSOI active area 134 by the formation of a mini-field oxidation (MFOX) 136". Forbes does not teach or suggest using oxygen implantation to form MFOX 136. Referring to column 8, lines 5-8, Forbes teaches "the MFOX 136 is also depicted in arbitrary shape and size. The actual size and shape of the MFOX 136 will be influenced by etch and oxidation conditions according to a process integration". Referring to paragraph [38] of Applicant's specification, "It has been discovered

that, all other conditions being equal, the same chips built on and across an SOI wafer do not display the same electrical and physical characteristics expected from them. Rather, the chips suffer performance loss due to leakage from the top silicon layer 6 to the silicon substrate 4 through the insulator layer 2. It has further been discovered that some performance losses can be avoided if the buried insulator layer 2 is purposefully not made flat. Thus, according to the present invention, the topography of the buried insulator layer 2 is patterned or altered to achieve a variety of advantages relative to the conventional, substantially flat buried oxide layer." For example, paragraphs [40 and 44] of Applicant's specification disclose performance improvement and decreased voltage breakdowns by changing the shape of insulator layer 2. Forbes does not teach or suggest changing the size and shape for MFOX 136 to improve performance. The size and shape of MFOX 136 are only "influenced by etch and oxidation conditions according to a process integration".

Referring to column 9, lines 38-44 and FIGS. 2A-2B, Forbes teaches processing a substrate 210 to form a strained Si/SiGe/SOI island and "an oxidation process is carried out to vertically isolate and SSOI active area 234 by the formation of a flattened mini-field oxidation (FMFOX) 236". Forbes does not teach or suggest using oxygen implantation to form FMFOX 236. Referring to column 9, lines 47-53, "Similar to the shape of the MFOX 136 (FIG. 1F), the size and shape of the FMFOX 236 is also depicted in arbitrary shape and size. The actual size and shape of the FMFOX 236 will be influenced by etch and oxidation conditions according to the placement of the upper deep implantation 209 and the lower deep implantation 211, their relative responses to a given etch recipe, and the extent of the oxidation process". Forbes does not teach or suggest changing the size and shape of FMFOX 236 to improve performance. The

size and shape of FMFOX 236 are only "influenced by etch and oxidation conditions according to the placement of the upper deep implantation 209 and the lower deep implantation 211".

With respect to amended claim 1, Yamagata does not disclose or suggest "forming an oxide insulator layer across the wafer by oxygen implantation, the insulator layer being buried within the silicon substrate, dividing the silicon substrate from a top silicon layer, and having a top surface and a bottom surface", "thickening the insulator layer by reducing one or more of the implantation dose, energy, and temperature", "creating at least one of a contoured top surface and a contoured bottom surface of the insulator layer by adjusting one or more of the implantation dose, energy, and temperature" and "annealing to further thicken and contour the insulator layer". Referring to column 4, lines 39-45 and FIG. 1B, Yamagata teaches preparing an SOI substrate 50 and subjecting a silicon thin film (a SOI layer) 3 on an insulating layer 4 of the SOI substrate to a wet-cleaning. The "wet-cleaning allows the thickness of the SOI layer to be decreased" to obtain a desired thickness. Insulator layer 4 is flat. Yamagata does not teach contouring a top surface or a bottom surface of insulator 4. Referring to column 6, lines 62-65 and FIG. 2H, Yamagata teaches performing hydrogen annealing "to obtain an SOI wafer comprising a 100 nm silicon layer and the 100 nm buried silicon oxide layer". Neither layer is thickened after annealing. Both layers remain flat after annealing. Referring to column 4, lines 48-50, Yamagata teaches constructing the SOI layer 3 "using a silicon thin film formed by the epitaxial growth or the hydrogen anneal. Yamagata does not teach annealing insulator layer 4. Yamagata does not teach thickening or contouring insulator layer 4.

Forbes and Yamagata, either separately or in combination, do not disclose or suggest "forming an oxide insulator layer across the wafer by oxygen implantation, the insulator layer being buried within the silicon substrate, dividing the silicon substrate from a top silicon

layer, and having a top surface and a bottom surface", "thickening the insulator layer by reducing one or more of the implantation dose, energy, and temperature", "creating at least one of a contoured top surface and a contoured bottom surface of the insulator layer by adjusting one or more of the implantation dose, energy, and temperature" and "annealing to further thicken and contour the insulator layer".

Accordingly, claim 1 as amended is believed to be patentable over Forbes in view of Yamagata. Therefore, reconsideration and withdrawal of the rejection with respect to this claim is respectfully requested and allowance of this claim is earnestly solicited.

Claims 4-5, 7-8 and 11-12 depend directly or indirectly from claim 1. Since claim 1 as amended is believed to be allowable, then claims 4-5, 7-8 and 11-12 are believed to be allowable as well for at least the reasons given hereinabove.

Applicant respectfully requests that the rejection of these claims be withdrawn and allowance of these claims is earnestly solicited.

Claim 14 has been amended in a manner believed to overcome the rejection. In particular, claim 14 has been amended to recite "forming an oxide insulator layer across the wafer by oxygen implantation, the insulator layer being buried within the silicon substrate, dividing the silicon substrate from a top silicon layer, and having a top surface and a bottom surface" and "thickening the insulator layer by reducing one or more of the implantation dose, energy, and temperature". Support is found at least in paragraphs [32-33, 35, 37, 42-43, 45-46, 48 and 52-54] and FIG. 8 of the specification and canceled claim 3.

Forbes does not disclose or suggest "forming an oxide insulator layer across the wafer by oxygen implantation, the insulator layer being buried within the silicon substrate, dividing the silicon substrate from a top silicon layer, and having a top surface and a bottom

surface", "thickening the insulator layer by reducing one or more of the implantation dose, energy, and temperature", "generating the chip periodicity for the wafer and setting the coordinates where a predetermined topography of the buried oxide insulator layer is desired", "transferring the coordinates to an oxygen implanter for implementation", "adjusting the energy, dose, or temperature of the oxygen implant with the implanter scanning and the wafer tilting or rotating according to preset coordinates from the chip periodicity map at the predetermined thicknesses and contours required, thereby creating at least one of a contoured top surface and a contoured bottom surface of the insulator layer" and " annealing to further thicken and contour the insulator layer". Referring to column 7, lines 46-51 and FIG. 1F, Forbes teaches processing a substrate 110 to form a strained Si/SiGe/SOI island. A bubble recess 132 is formed by an isotropic etch and "an oxidation process is carried out to vertically isolate an SSOI active area 134 by the formation of a mini-field oxidation (MFOX) 136". Forbes does not teach or suggest using oxygen implantation to form MFOX 136. Referring to column 8, lines 5-8, Forbes teaches "the MFOX 136 is also depicted in arbitrary shape and size. The actual size and shape of the MFOX 136 will be influenced by etch and oxidation conditions according to a process integration". Forbes does not teach or suggest changing the size and shape for MFOX 136 to improve performance. The size and shape of MFOX 136 are only "influenced by etch and oxidation conditions according to a process integration". Referring to column 9, lines 38-44 and FIGS. 2A-2B, Forbes teaches processing a substrate 210 to form a strained Si/SiGe/SOI island and "an oxidation process is carried out to vertically isolate and SSOI active area 234 by the formation of a flattened mini-field oxidation (FMFOX) 236". Forbes does not teach or suggest using oxygen implantation to form FMFOX 236. Referring to column 9, lines 47-53, "Similar to the shape of the MFOX 136 (FIG. 1F), the size and shape of the FMFOX 236 is also depicted in

arbitrary shape and size. The actual size and shape of the FMFOX 236 will be influenced by etch and oxidation conditions according to the placement of the upper deep implantation 209 and the lower deep implantation 211, their relative responses to a given etch recipe, and the extent of the oxidation process". Forbes does not teach or suggest changing the size and shape of FMFOX 236 to improve performance. The size and shape of FMFOX 236 are only "influenced by etch and oxidation conditions according to the placement of the upper deep implantation 209 and the lower deep implantation 211".

Yamagata does not disclose or suggest "forming an oxide insulator layer across the wafer by oxygen implantation, the insulator layer being buried within the silicon substrate, dividing the silicon substrate from a top silicon layer, and having a top surface and a bottom surface", "thickening the insulator layer by reducing one or more of the implantation dose, energy, and temperature", "generating the chip periodicity for the wafer and setting the coordinates where a predetermined topography of the buried oxide insulator layer is desired", "transferring the coordinates to an oxygen implanter for implementation", "adjusting the energy, dose, or temperature of the oxygen implant with the implanter scanning and the wafer tilting or rotating according to preset coordinates from the chip periodicity map at the predetermined thicknesses and contours required, thereby creating at least one of a contoured top surface and a contoured bottom surface of the insulator layer" and "annealing to further thicken and contour the insulator layer". Referring to column 4, lines 39-45 and FIG. 1B, Yamagata teaches preparing an SOI substrate 50 and subjecting a silicon thin film (a SOI layer) 3 on an insulating layer 4 of the SOI substrate to a wet-cleaning. The "wet-cleaning allows the thickness of the SOI layer to be decreased" to obtain a desired thickness. Insulator layer 4 is flat. Yamagata does not teach contouring a top surface or a bottom surface of insulator 4. Referring to column 6, lines

62-65 and FIG. 2H, Yamagata teaches performing hydrogen annealing "to obtain an SOI wafer comprising a 100 nm silicon layer and the 100 nm buried silicon oxide layer". Neither layer is thickened after annealing. Both layers remain flat after annealing. Referring to column 4, lines 48-50, Yamagata teaches constructing the SOI layer 3 "using a silicon thin film formed by the epitaxial growth or the hydrogen anneal. Yamagata does not teach annealing insulator layer 4. Yamagata does not teach thickening or contouring insulator layer 4.

Forbes and Yamagata, either separately or in combination, do not disclose or suggest "forming an oxide insulator layer across the wafer by oxygen implantation, the insulator layer being buried within the silicon substrate, dividing the silicon substrate from a top silicon layer, and having a top surface and a bottom surface", "thickening the insulator layer by reducing one or more of the implantation dose, energy, and temperature", "generating the chip periodicity for the wafer and setting the coordinates where a predetermined topography of the buried oxide insulator layer is desired", "transferring the coordinates to an oxygen implanter for implementation", "adjusting the energy, dose, or temperature of the oxygen implant with the implanter scanning and the wafer tilting or rotating according to preset coordinates from the chip periodicity map at the predetermined thicknesses and contours required, thereby creating at least one of a contoured top surface and a contoured bottom surface of the insulator layer" and " annealing to further thicken and contour the insulator layer".

Accordingly, claim 14 as amended is believed to be patentable over Forbes in view of Yamagata. Therefore, reconsideration and withdrawal of the rejection with respect to this claim is respectfully requested and allowance of this claim is earnestly solicited.

Rejection of Claims 2, 6, 9-10 and 13 under 35 U.S.C. § 103(a)

Claims 2, 6, 9-10 and 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Forbes and Yamagata as applied to claim 1 above, and further in view of Peckerar et al. (U.S. Patent No. 6,309,934), hereinafter "Peckerar".

Claims 2, 6, 9-10 and 13 depend directly or indirectly from claim 1. Since claim 1 as amended is believed to be allowable, then claims 2, 6, 9-10 and 13 are believed to be allowable as well for at least the reasons given hereinabove.

Applicant respectfully requests that the rejection of these claims be withdrawn and allowance of these claims is earnestly solicited.

Conclusion

In view of the foregoing amendments and remarks, Applicant respectfully submits that all claims now pending in this application, namely Claims 1-2 and 4-14 are now in condition for allowance. Accordingly, early and favorable consideration of this application is respectfully requested. Should the Examiner believe that a telephone or personal interview may facilitate resolution of any remaining matters, he is respectfully requested to contact Applicant's undersigned attorney at the telephone number indicated below.

No fee is believed to be due for the submission of this amendment. If any fees are required, however, the Commissioner is authorized to charge such fees to Deposit Account No. 09-0458.

Respectfully Submitted,

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